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## APPLICANTS

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\*\* CONTINUING DATA \*\*\*\*\*

*none*

\*\* FOREIGN APPLICATIONS \*\*\*\*\*

JAPAN 2002-281842 09/26/2002

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IF REQUIRED, FOREIGN FILING LICENSE GRANTED

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Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	STATE OR COUNTRY JAPAN	SHEETS DRAWING 6	TOTAL CLAIMS 11	INDEPENDENT CLAIMS 2
35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	EXAMINER'S SIGNATURE <i>hl</i>	INITIALS		
Verified and Acknowledged				

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## TITLE

Phase-locked loop circuit reducing steady state phase error

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